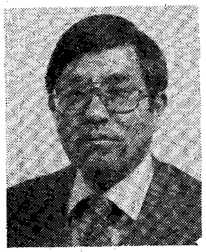

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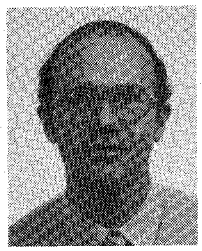

Paul Saunier (M'74) was born in France in 1950. He received the Diplome d'Ingenieur from the Ecole Centrale de Lyon, Lyon, France, in 1973, and the Ph.D. degree in electrical engineering from Carnegie-Mellon University, Pittsburgh, PA, in 1979, where he studied the electrooptic light modulation in $LiNbO_3$ waveguiding structures.

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Design of Broad-Band Power GaAs FET Amplifiers

YUSUKE TAJIMA MEMBER, IEEE, AND PATRICK D. MILLER

Abstract — **A model is presented for the drain–gate breakdown phenomenon of GaAs FET's, based on experimental results. This breakdown model is added to a previously published large-signal model and incorporated in a powerful computer-aided design program called LSFET. The program is capable of searching for the optimum power load for an FET and simulating the power performance of multistage amplifiers. The design of power amplifiers is discussed in detail, using the knowledge gained from LSFET. Data is presented from a fabricated monolithic broad-band power amplifier chip showing good agreement between measured results and simulated curves.**

I. Introduction

REQUIREMENTS to design an amplifier with the best gain and power performance in a wide frequency band necessitate a different approach and technology from the design of narrow-band amplifiers. First, a large-signal FET model has to be developed in order to predict the power saturation correctly. This model should not require a time-consuming data-taking technique as in the load-pull method, but still has to be comprehensive and capable of generating large-signal parameters under any bias voltage, RF signal levels, and any load conditions. Secondly, it is important to have an understanding of the interaction between the circuits and FET's in order to realize the best compromise between the gain, power, ripple, and bandwidths. Few papers have discussed these problems previously.

Some studies have been published on large-signal models of GaAs FET's, in which the nonlinear behavior of g_m and G_d, as well as the forward gate current, were discussed [1]–[3]. However, the gate breakdown was never modeled based on experimental data, though it is considered one of the important power-limiting mechanisms of FET's. We will first describe the experimental results of the breakdown phenomenon and then discuss its implementation in the large-signal model described in the previous paper [1].

In the next section, we will demonstrate the application of this large-signal model to a broad-band power amplifier design. A CAD program that simulates and predicts the

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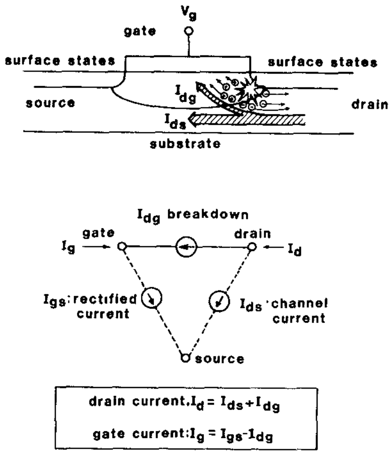

Fig. 1. Current flow within an FET.

power gain performance of multistage amplifiers was developed. It will be seen that the power saturation mechanisms can vary in the frequency band. A design procedure which will give the best gain/power compromise will be discussed.

Finally, the actual fabrication of a two-stage monolithic amplifier is described. Its performance will be compared with the design goals.

II. Breakdown Model

The FET breakdown takes place at the edge of a gate finger close to the drain where the highest field is applied. A light emission can be observed at this location at the onset of the breakdown. The breakdown current is due to the generation of electron-hole pairs. The hole current, when it exists, is collected at the gate terminal where the deepest potential voltage is usually applied. Thus, breakdown current I_{dg} will flow from drain to gate as indicated by a solid line in Fig. 1. Other currents that flow in an FET structure are the channel current I_{ds} between drain and source, and the gate rectified current I_{gs} between gate and source. The latter exists only when the FET is under large-signal operation.

Drain current I_d consists of two currents, channel current I_{ds} and breakdown current I_{dg}. Drain current I_d of an FET with 1600-μm total gate periphery was measured and is shown in Fig. 2(a). The breakdown current I_{dg} also was measured at the gate terminal and is shown in Fig. 2(b). Net current $I_d - I_{dg}$ is the channel current I_{ds} which is shown in Fig. 2(c).

In Fig. 3, the breakdown current I_{dg} was replotted on a chart with the voltage difference V_{dg} between drain and gate as a parameter. It shows that once the FET is pinched off $V_g \leqslant V_p$, the gate and drain terminals become isolated from the source terminal, and the breakdown characteristics are determined only by the voltage difference between gate and drain. When the channel is not pinched-off $V_g > V_p$, the breakdown characteristics become a strong function of channel current I_{ds} (or gate voltage V_{gs}).

This breakdown behavior is considered to be due to the formation of a dipole layer behind the depletion layer near the drain (Fig. 4). A dipole layer absorbs part of the voltage drop across drain and gate, thereby easing the field accumulation near the gate edge and increasing the total voltage drop between gate and drain before going to breakdown. Thus, the breakdown voltage will be higher with the existence of the domain, whose size is a function of the channel current. The larger the channel current, the

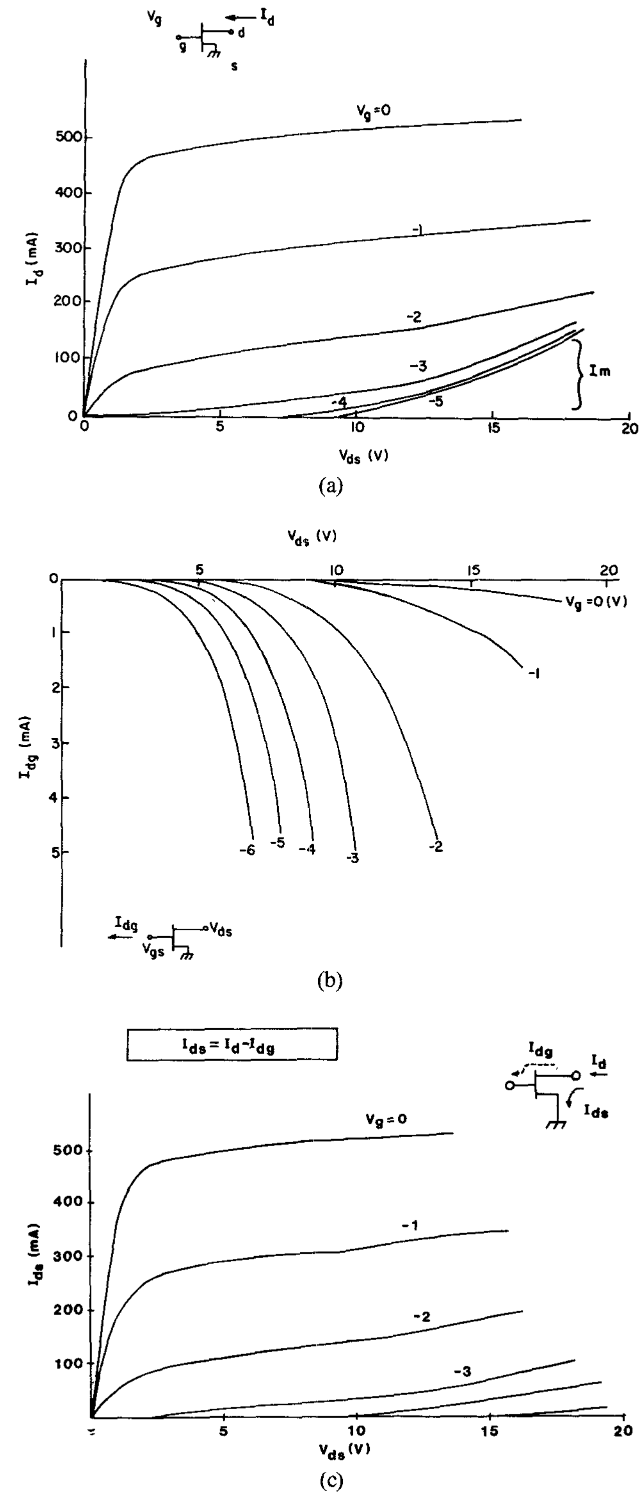

Fig. 2. (a) Measured drain current characteristics for 1.6-mm FET. (b) Breakdown current as a function of drain–source voltage. (c) Channel current as a function of drain–source voltage.

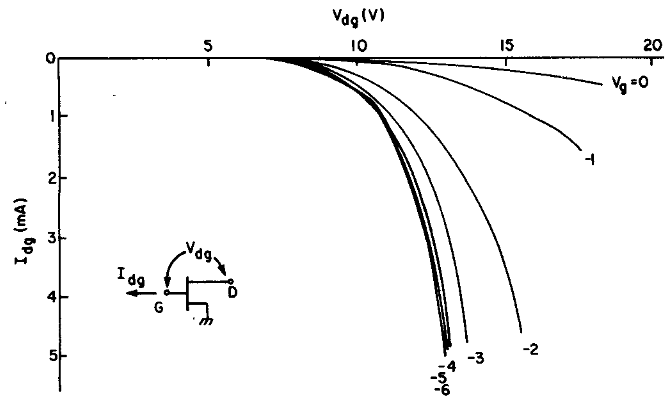

Fig. 3. Breakdown current as a function of drain–gate voltage.

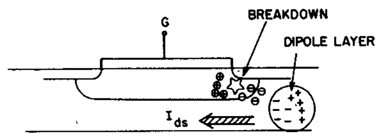

Fig. 4. Formation of dipole layer at gate–drain junction.

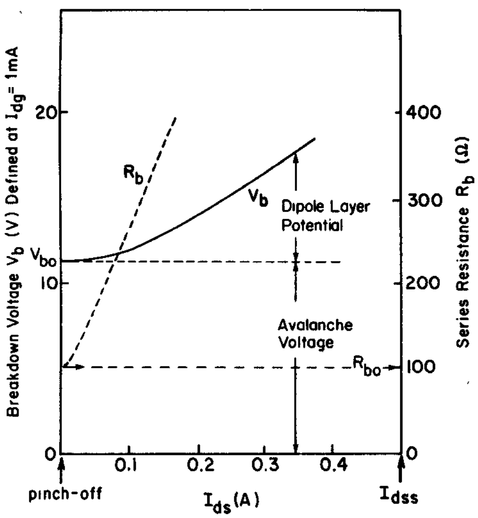

Fig. 5. Drain–gate breakdown voltage and resistance as a function of channel current.

larger the domain, resulting in a higher breakdown voltage and a larger series resistance.

Breakdown currents in Fig. 3 were simulated by the following equations with parameters V_b (breakdown voltage) and R_b (series resistance) as dependent variables of I_{ds}:

$$I_{dg} = 0, \qquad V_{dg} < V_b$$
$$I_{dg} = \frac{1}{R_b}(V_{dg} - V_b), \qquad V_{dg} > V_b. \tag{1}$$

As plotted in Fig. 5, V_b and R_b increase almost linearly with I_{ds}. The difference between V_b and V_{b0} (breakdown voltage when $I_{ds} = 0$) is the voltage drop in the dipole layer. For the purpose of the large-signal simulation, V_b and R_b were approximated by the following equations:

$$V_b = V_{b0} + R_1 I_{ds}$$
$$R_b = R_{b0} + R_2 \cdot (I_{ds}/I_{dss}). \tag{2}$$

Using (1) and (2), four parameters, V_{b0}, R_{b0}, R_1, and R_2, can describe the breakdown current at any bias condition, provided the channel current I_{ds} is also derived by the bias condition.

Current models for I_{ds} and I_{gs} are already described in [1]. More parameters were added to make the simulation fit better to measured curves. The resulting equations are given in the Appendix. Using these equations, all the currents in the FET can be calculated at any given terminal voltage condition. Fig. 6 shows an example of simulated drain current which was obtained by superimposing simulated breakdown current on the channel current. The similarity of these curves to measured ones in Fig. 2(a) is excellent.

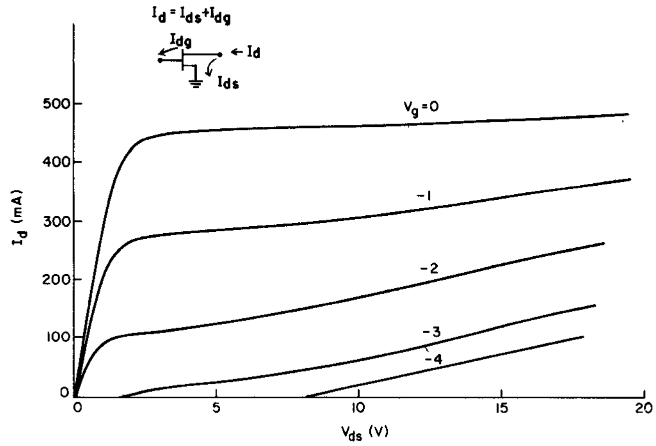

Fig. 6. Simulated drain current characteristics.

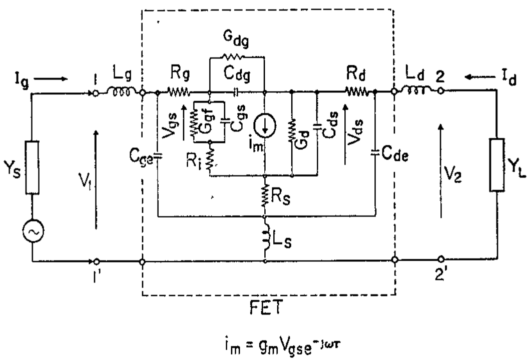

Fig. 7. Large-signal FET model.

III. Large-Signal Model

The large-signal model [1] was upgraded by adding the breakdown conductance (G_{dg}) between drain and gate, in parallel with gate–drain capacitance C_{dg} (Fig. 7). This nonlinear value was calculated from the instantaneous voltage difference $V_{dg}(t)$ at gate and drain, which was used to derive a breakdown current wave form $I_{dg}(t)$. This calculation requires a few iterations until the circuit condi-

FREQUENCY(GHZ)= 16.00 OPTIMIZATION

SMALL SIGNAL PERFORMANCE

	S11(MAG,DEG)		S12(MAG,DEG)		S21(MAG,DEG)		S22(MAG,DEG)		MAG MSG(DB)	K	S21(DB)
AMPLIFIER S PARA	.853E+00	-.163E+03	.566E-01	.347E+02	.790E+00	.390E+02	.583E+00	-.116E+03	7.132	1.536	-2.044

LARGE SIGNAL PERFORMANCE

PIN (DBM)	POUT (DBM)	GAIN (DB)	PAE (PCENT)	GGF (S)	CGS (PF)	RI (OHM)	GM (S)	GD (S)	GDG (S)	IDS (MA)	IDG (MA)	IGS (MA)	YSC (MS)		YLD (MS)	
0.00	0.00	0.00	0.00	.28E-28	.97E+00	.12E+01	.90E-01	.83E-02	0.	180.	0.00	.00	38.72	-125.13	9.22	-30.86
-.68	7.07	7.75	.29	.44E-27	.97E+00	.12E+01	.91E-01	.83E-02	0.	180.	0.00	.00	42.07	-123.75	10.96	-29.12
5.36	13.16	7.79	1.19	.65E-25	.98E+00	.12E+01	.92E-01	.83E-02	0.	181.	0.00	.00	42.15	-124.01	10.94	-29.13
8.91	16.72	7.81	2.69	.14E-22	.98E+00	.12E+01	.92E-01	.83E-02	0.	182.	0.00	.00	42.35	-124.41	10.92	-29.11
11.43	19.25	7.82	4.76	.38E-20	.98E+00	.12E+01	.92E-01	.83E-02	0.	184.	0.00	.00	42.65	-124.99	10.90	-29.08
13.41	21.22	7.82	7.40	.11E-17	.99E+00	.12E+01	.93E-01	.83E-02	0.	187.	0.00	.00	43.07	-125.77	10.88	-29.03
15.04	22.85	7.82	10.57	.34E-15	.10E+01	.12E+01	.93E-01	.83E-02	0.	190.	0.00	.00	43.62	-126.78	10.86	-28.97
16.46	24.20	7.73	14.20	.11E-12	.10E+01	.12E+01	.94E-01	.83E-02	.60E-04	192.	.25	.00	44.86	-127.55	11.02	-28.79
17.77	25.26	7.49	17.77	.36E-10	.10E+01	.12E+01	.93E-01	.83E-02	.15E-03	194.	[illegible]	.00	47.43	-125.72	13.43	-28.35
18.92	26.12	7.20	21.27	.12E-07	.10E+01	.11E+01	.93E-01	.83E-02	.27E-03	195.	1.26	.00	49.76	-125.01	15.58	-28.07
19.99	26.85	6.85	24.25	.42E-05	.11E+01	.11E+01	.93E-01	.83E-02	.38E-03	198.	1.82	.00	52.47	-125.11	18.14	-27.70
21.15	27.49	6.34	26.83	.15E-02	.11E+01	.11E+01	.93E-01	.83E-02	.47E-03	201.	2.31	1.62	57.34	-125.89	20.40	-27.22
23.68	27.88	4.20	23.51	.28E-01	.11E+01	.11E+01	.92E-01	.83E-02	.53E-03	202.	2.66	31.86	80.09	-106.94	22.01	-25.98
28.14	28.39	.25	2.42	.12E+00	.11E+01	.10E+01	.92E-01	.83E-02	.62E-03	202.	3.22	141.27	127.79	-51.41	24.00	-24.77
36.11	29.80	-6.30	******	.52E+00	.12E+01	.10E+01	.93E-01	.83E-02	.96E-03	206.	5.58	626.46	186.73	57.83	33.97	-22.87

READY.

Fig. 8. Sample output from LSFET (optimization mode).

tion converges at a stable point. The fundamental component of $I_{dg}(t)$ was used to calculate the resistive component G_{dg}.

A multipurpose large-signal program, LSFET, was developed, based on this nonlinear equivalent circuit model. Derivation of other nonlinear components was described in [1]. Because it uses the frequency domain analysis, computation time is very reasonable, which makes it capable of 1) searching for the optimum load condition for a given FET, and 2) simulating the power performance of single or multistage amplifiers. It is user-friendly because:

1) It calls the data library for necessary FET parameter values by identification labels. Each FET data file contains 28 parameters for complete characterization of the linear and nonlinear elements. These elements are measured beforehand and stored with a label, which is called by LSFET when necessary.

2) Matching circuits in the amplifier simulation are filed separately. They have an identical format that is used in COMPACT. This allows for any complication in the matching circuit as long as COMPACT can calculate Y-parameters, and enables designers to use COMPACT for designing and optimizing the circuit. After a circuit is designed, LSFET can take over the circuit files to simulate the power performance.

3) Results are obtained by printout and/or graphics, in a form convenient to the user. The program can be called by various users, once the necessary circuit files are stored in their own library.

Fig. 8 shows the printout of the optimization mode in which the optimum load impedance is calculated for a swept input power level from -0.68–36 dBm. Columns YSC and YLD show the optimum admittances that give the best gain at the particular input level. As the input level increases, these admittances change from the small-signal optimum to large-signal optimum. The best power condition is found when the power-added efficiency (PAE) is at its maximum (underlined).

Columns GGF to GDG show the values of the nonlinear elements in the equivalent circuit in Fig. 7 while I_{dg}, I_{ds}, and I_{gs} are the currents between terminals shown in Fig. 1. Changes in these currents indicate different saturation modes of the FET. For example, an increase in I_{dg} is due to the breakdown, while an increase in I_{gs} is due to the RF forward swing at the gate. The net gate current observed at the gate terminal is the difference between I_{dg} and I_{gs}, i.e., $I_g = I_{gs} - I_{dg}$.

LSFET results for an amplifier simulation also have a similar printout to Fig. 8 for each specified frequency. When more than two FET's are cascaded in a multistage amplifier, only the last two stages are assumed to be driven into a large-signal condition. The program iterates the calculation until circuit conditions are satisfied for both of the FET's. Some of the information found in the printout is small-signal gain, saturation power, 1-dB compression power, power-added efficiency, and the saturation mode of the amplifier at every frequency point. As will be discussed in the next section, the saturation of an amplifier can be complicated, especially in the case of multistage amplifiers.

IV. Design of a Broad-Band Power Amplifier

The first step in the power amplifier design would be to realize the output matching circuit to meet the optimum power condition in a given frequency band. The optimum power condition is calculated by LSFET using its optimization mode. The frequency locus of this power condition, where power-added efficiency is maximized at every frequency, generally takes a constant conductance line as shown in Fig. 9. If stability factor k is larger than 1, the FET's maximum small-signal gain condition also takes a constant conductance locus, where its conductance G_g is smaller than that for the power condition G_p. This situation is easily seen from the schematic $I-V$ curve in Fig. 10. The maximum power condition is shown by load line a, while the maximum gain condition is obtained from a load line having negative the slope of dotted line g, which is tangent to the $I-V$ curve at the bias point. The difference of the slopes of a and g always makes $G_p > G_g$.

Another significant difference between optimum gain and power conditions is that the maximum gain varies with

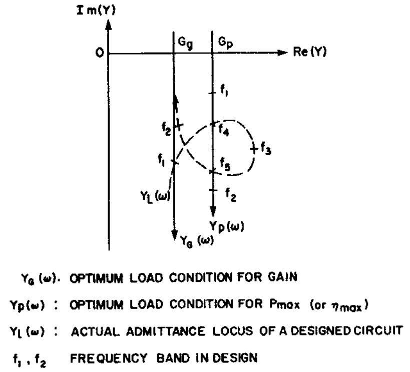

Fig. 9. Optimum gain versus optimum power with a typical admittance locus.

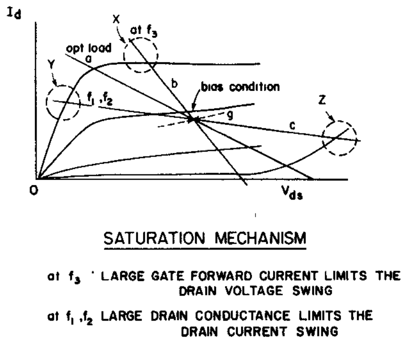

Fig. 10. Saturation mechanisms associated with different load lines.

frequency, but the power stays fairly constant up to the frequency range, where a dephasing effect starts to affect the power-combining efficiency from many cells.

The goal of matching circuit designs is to realize the locus of optimum load condition within a given frequency band, but this is generally very difficult. An offset from this condition causes an early saturation. If the actual load G is larger than G_p, and the load line is given by b in Fig. 10, power saturation will start to take place by the overswing of the RF voltage into the forward region of the gate–source junction, as shown by region X in the figure. The power saturation mechanism in this case is the gate forward current which increases the loss G_{gs} in the input terminal. On the other hand, if the actual load G is smaller than G_p, the power saturates due to the overswing into the ohmic region Y or the breakdown region Z, as indicated by load line c. An increase in G_{ds}, G_{gd}, and breakdown current I_{dg} will be observed in this case. Thus, we can divide the admittance chart in Fig. 9 into two saturation mode regions, breakdown saturation mode for $G < G_p$ and forward gate current saturation for $G > G_p$.

The loci of the optimum condition and the actual load move in opposite directions. The matching elements can introduce a loop or loops in the load line and realize a matching between the two loci locally. By adding circuit elements, the number of loops increases and the broad-band matching improves. In a practical design, the number of elements is limited by chip-size considerations and circuit losses.

Let us suppose one loop was made on the matching circuit. In order to stay in the vicinity of the power

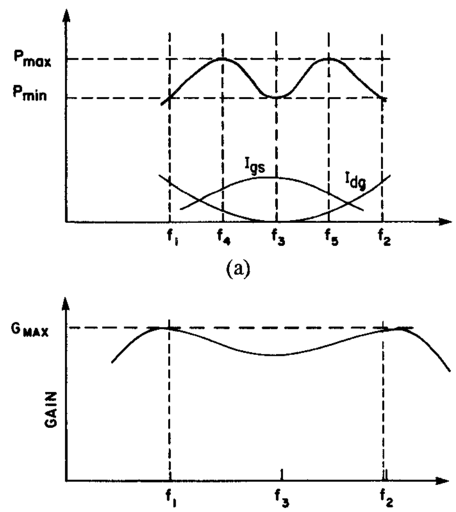

Fig. 11. (a) Saturation power and (b) small-signal gain of a typical power amplifier.

condition, the loop in the load line was designed as shown by the dotted line in Fig. 9. At frequencies f_4 and f_5, the circuit can exhibit the optimum load, while at other frequencies, the output power will be less. Thus, it is expected that the power performance will have a frequency dependency as shown in Fig. 11, with a slight dip at frequency f_3. Between f_4 and f_5, the circuit will be saturated by the gate current, while at other frequencies by the breakdown current. Gate current at saturation is also shown in the figure, indicating these changes in saturation modes with frequency.

Another implication of Fig. 9 is that the load line stays in the vicinity of the gain optimum in a wider frequency region than it does for the power optimum. Thus, it brings a wider bandwidth for small-signal gain than for the power, as shown in Fig. 11, which is typically seen in actual amplifiers. A power amplifier has to be designed for wider small-signal bandwidth than required.

The design of a two-stage amplifier is more complicated. The power condition has to be met for the first-stage FET as well as for the second, in order to guarantee that the second-stage FET is driven sufficiently by the first-stage. A failure to do this can cause an early saturation in the first stage, leaving the second stage at a low driving level. For a broad-band amplifier, the power match at the first stage becomes increasingly difficult. One way to obtain sufficient power to drive the second stage even with a poor match is to increase the total gate periphery of the first-stage FET. This situation is monitored during the course of designing the amplifier by the increase in I_{dg} and/or I_{gs} of each FET in LSFET printouts. Proper design of the interstage circuit and proper choice of FET size for the two stages both are important results that can be derived from the LSFET design. The best combination of FET size for two stages becomes a function of the bandwidth, gain of FET's, matching circuits, etc.

Finally, input circuit designs are performed to achieve the best small-signal gain flatness in the band. All the

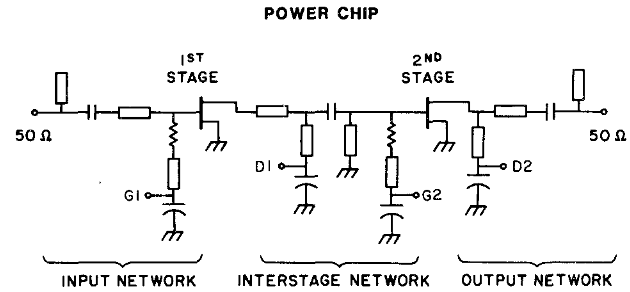

Fig. 12. Circuit topology for monolithic power amplifier.

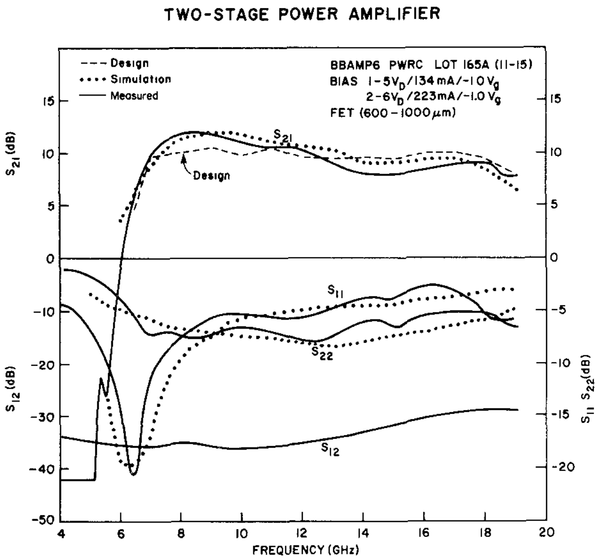

Fig. 13. Measured small-signal performance of single-ended amplifier chip.

undesirable gain ripple resulting from the power design should be smoothed out by the input circuit. If this is difficult, the power condition may have to be compromised.

As we described above, the power amplifier design, especially that for the multistage broad-band application, is a complicated procedure which cannot be performed without a computer simulation program capable of calculating the power performance of FET's under any circuit or driving conditions.

V. Amplifier Performance

A monolithic broad-band amplifier was actually designed following the technique discussed above. The circuit was designed for the 7–18-GHz band, 10-dB gain, and 400-mW output power. The size of FET's was chosen to be 0.6 mm driving 1.0 mm. Some of the small-signal device parameters for the 1.0-mm FET are: $C_{gs} = 1.0$ pF, $g_m = 100$ mS, $G_d = 8.3$ mS, $C_{dg} = .075$ pF, $C_{ds} = 0.24$ pF.

The circuit topology is shown in Fig. 12. Thin-film Si_3N_4 capacitors, on the order of 1 pF, are used for impedance matching and dc isolation. Larger capacitors, 7–10 pF, are used for RF bypass enabling the FET's to be biased through the shorted stubs.

Resistive loading is used at the gate of each FET to absorb excess gain and stabilize the circuit at the low end of the band. This shunt conductance is essential in the interstage network where the impedance mismatch is extreme and the power matching critical.

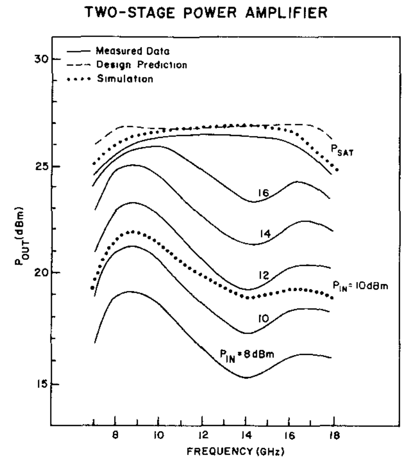

Fig. 14. Measured power performance of amplifier chip versus LSFET simulation.

As explained in the previous section, the output and interstage networks are designed to realize the power optimum load at the drains of the second- and first-stage FET's, respectively. The input stage is designed to achieve 9 to 10 dB of small-signal gain across the frequency band.

This two-stage power amplifier was fabricated on 0.1-mm GaAs with vapor phase-deposited epilayers. The carrier density was $1.7 \times 10^{17}/cm^3$, with 0.8–0.9-μm gates. Total gate periphery is 1.6 mm, with final chip dimensions of 0.093 in by 0.075 in.

Small-signal results for the single-ended chip are in Fig. 13 and show 8–12 dB of gain from 7–18 GHz. The power performance is shown in Fig. 14. Output power is greater than 315 mW (25 dBm), with 7.0 dB to 8.5 dB associated gain from 7.5–17 GHz. The circuit output over 400 mW (26 dBm) of power, with greater than 6-dB associated gain from 9–16 GHz.

To simulate the test results, gate–source capacitances were increased, microstrip bends were taken into account, and distributed effects were added to the lumped capacitors. Figs. 13 and 14 include the simulation for both small- and large-signal results. These plots show the ability of the large-signal modeling and LSFET program to predict the power performance of a multistage amplifier. The discrepancy in the absolute power level is mainly due to jig losses not being removed from the measurement. However, the simulation bandwidth matches very well the measured power bandwidth of the fabricated circuit.

VI. Conclusion

The large-signal model developed in an earlier paper was upgraded by adding a breakdown model. This made the model comprehensive, capable of predicting saturation mechanisms at various conditions.

A multi-purpose, user-friendly program called LSFET was developed. The program calculates the power performance of an FET or a multistage amplifier and predicts the saturation modes.

Using the results of LSFET, the general problems which are found in a broad-band power amplifier design were discussed. It was demonstrated that the saturation mechanism can vary in the frequency band, that the power bandwidth is usually smaller than the gain bandwidth, and that in two-stage amplifiers, early saturation by the first stage can be avoided by the proper choice of FET's and good interstage design.

Finally, results from a two-stage monolithic amplifier were demonstrated.

Appendix

The following equations are used in LSFET to calculate the channel current I_{ds} as a function of V_{ds} and V_{gs}:

$$I_{ds} = I_{DSS} F_G F_D + G_{DO} V_{ds}$$

$$F_G = \frac{1}{K}\left[V_{GSN} - \left(\frac{1-\exp(-mV_{GSN})}{m}\right)\right]$$

$$F_D = 1 - \exp - \left(V_{DSN} + aV_{DSN}^2 + bV_{DSN}^3\right)$$

$$V_{GSN} = 1 + \frac{V_{gs}}{V_p}$$

$$V_{DSN} = \frac{V_{ds}}{V_{DSP}\left(1 + \frac{wV_{GS}}{V_p}\right)}$$

$$V_P = V_{PO} + pV_{ds}$$

$$K = 1 - \frac{1-\exp(-m)}{m}.$$

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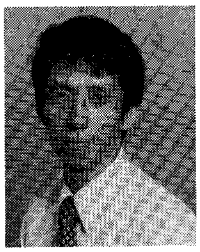

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